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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,254	02/12/2004	Yasuyuki Hori	1460.1045	4159

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EXAMINER	
SCHLIE, PAUL W	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,254	HORI, YASUYUKI	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, and 6-9 have been examined as amended, with claim 5 being canceled.

Response to Arguments

2. Applicant's arguments filed 6/19/06 have been fully considered but they are not persuasive and/or moot in view of their clarified rejection.

As although argued otherwise, both the claimed invention and that taught by Thankrakul enable a reprogrammable non-volatile memory; accessible as a source program memory when operating in a normal mode enabled by a first chip select, or alternatively accessible as a destination data memory when operating in a re-program/re-write mode enabled by a second chip select in lieu of a volatile memory otherwise being accessible by said second chip select when operating in a normal mode (see figure 7, "RDMCS* signal, To Microprocessor Flash/EEPROM Memory")

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Thantrakul (5,784,611).

As per independent claim 1, Thantrakul teaches a microcontroller system and/or method comprising: an embedded processor; a potential plurality of addressable internal and/or external volatile and non-volatile memories within which may themselves contain non-volatile reprogramming code (see figures 6-11); and reprogramming logic comprising an external mode select signal (see ISPA* in figure 7) where upon detection of said mode select after reset, said logic may be configured to logically remap said memories (and/or inherently regions of said memories) to enable the execution of said reprogramming code and logical access to target reprogrammable memory as may be required to enable it's sequential reprogramming from some data source by said embedded processor (see figure 8). Correspondingly the logic in (figure 7) clearly depicts a circuit enabling a reprogrammable non-volatile memory; accessible as a source program memory when operating in a normal mode enabled by a first chip select, or alternatively accessible as a destination data memory when operating in a re-program/re-write mode enabled by a second chip select in lieu of a volatile memory otherwise being accessible by said second chip select when operating in a normal mode (see figure 7, "RDMCS* signal, To Microprocessor Flash/EEPROM Memory")

As per claims 2-3 and 7-9, being dependant on claim 1, or correspondingly dependent claim inclusively, Thantrakul further teaches that said reprogramming code may be transferred from its initial storage/source location to volatile memory prior to executing said reprogramming code from said volatile memory (see figure 9A), and

enables the selection of an initial logical address mapping of said memories upon power-on/reset (see figure 8).

Where although the terminology utilized by the reference may differ from that claimed, all limitations within claims 1-3 and 7-9 are considered clearly taught, and thereby known to those of ordinarily skill in the art at the time of the claimed invention.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 4 and 6 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. As elements critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

As per claims 4 and 6, as the circuitry/logic required to enable a microprocessor to seamlessly transition program execution to a reprogrammed non-volatile memory by outputting a mode switch signal upon completing the re-writing of said non-volatile memory as implicitly required by that claimed is provided within the disclosure; the claims are not considered sufficiently enabled.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765, or email address [paul.schlie@uspto.gov]. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
8/2/06